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## HP E2448A

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| 1. Did you receive your product when expected? | [ ] | [ ] |
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_____

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_____

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_____

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_____

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**Manufacturer's Name:** Hewlett-Packard Company

**Manufacturer's Address:** 1900 Garden of the Gods Road
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U.S.A.

**Declares, That the product**

**Product Name:** 68360 Preprocessor Interface

**Model Number(s):** HP E2448A

**Product Options:** All

**Conforms to the following Product Specifications:**

**Safety:** IEC 348 / HD 401
UL 1244
CSA - C22.2 No. 231 Series M-89

**EMC:** CISPR 11:1990 /EN 55011 (1991): Group 1 Class A
IEC 801-2:1991 /EN 50082-1 (1992): 4 kV CD, 8 kV AD
IEC 801-3:1984 /EN 50082-1 (1992): 3 V/m
IEC 801-4:1988 /EN 50082-1 (1992): 1 kV

**Supplementary Information:**
The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC.

Colorado Springs, July 5, 1993

John Strathman, Quality Manager

European Contact: Your local Hewlett-Packard Sales and Service Office or Hewlett-Packard GmbH, Department ZQ / Standards Europe, Herrenberger Strasse 130, 71034 Böblingen Germany (FAX: +49-7031-143143)

# HP E2448A Motorola 68360 Preprocessor Interface User's Guide

**for the HP 1660A/61A and HP 16550A Logic Analyzers**




Manual Part Number E2448-97002 Printed in U.S.A. July 1994

## Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software code may be printed before the date; this indicates the version of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Edition 1 July 1994 E2448-97002

## List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in the Printing History and on the title page.

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# Contents

## Chapter 3: General Information



## Appendix A: Troubleshooting

# Introduction

The HP E2448A Preprocessor Interface provides a complete interface for state or timing analysis of a Motorola 68360 target system by an HP 1660A/61A or HP 16550A Logic Analyzer. It also provides a 10-pin BDM connector for connecting a BDM (Background Debug Mode) debugger to the preprocessor interface.

The 68360 configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the 68360 microprocessor. It also loads the inverse assembler for obtaining displays of 68360 data in 68360 assembly language mnemonics.

## Logic Analyzers Supported

The following logic analyzers are supported by the HP E2448A:

### HP 1660A/61A

The HP 1660A/61A Logic Analyzers provide 4 k of memory depth with 136 channels (HP 1660A) or 102 channels (HP 1661A) of 100 MHz state analysis or 250 MHz timing analysis. These logic analyzers also support various combinations of mixed state/timing analysis.

### HP 16550A (one or two cards)

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz timing analysis. This logic analyzer also supports various combinations of mixed state/timing analysis.

**Note** 

The HP E2448A contains eleven 16-channel pods, six of which are required for inverse assembly with state analysis. Only the HP 16550A Logic Analyzer (two cards) has sufficient channels to monitor all eleven pods simultaneously.

## Logic Analyzer Software Requirement

The HP E2448A Preprocessor Interface requires HP 16500A system and module software version V05.03 or higher for the HP 16550A Logic Analyzer. For the HP 16500B mainframe, system and module software version V01.00 or higher is required. For the HP 1660A/61A Logic Analyzers, software version V01.00 or higher is required. To use the enhanced inverse assembler with the HP 1660A/61A Logic Analyzers, software version V02.00 or higher is required. If your software version is older than those listed above, load new system software with the above version numbers or higher before loading the HP E2448A software.

## How to Use This Manual

This manual is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP E2448A Preprocessor Interface for state or timing analysis with the supported logic analyzers.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP E2448A software. It also provides information about the inverse assemblers and status encoding.
- Chapter 3 contains additional reference information including the characteristics and signal mapping for the HP E2448A Preprocessor Interface. It also contains information on servicing.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

# 1

# Setting Up the HP E2448A

## Introduction

This chapter explains how to install and configure the HP E2448A Preprocessor Interface for state or timing analysis with the supported logic analyzers.

## Duplicating the Master Disk

Before you use the HP E2448A software, use the Duplicate Disk operation in the disk menu of your logic analyzer to make a duplicate copy of the HP E2448A master disk. Store the master disk in a safe place and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

## Equipment Supplied

The HP E2448A Preprocessor Interface consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor interface circuit card and cables.
- The configuration and inverse assembly software on a 3.5-inch disk.
- This user's guide.

**Note**

The preprocessor interface socket assembly pins are covered at the time of shipment with either a conductive foam wafer or a conductive plastic pin protector. This is done to protect the delicate gold plated pins of the assembly from damage due to impact.

When you're not using the preprocessor interface, protect the socket assembly pins from damage by covering them with the foam or plastic pin protector.

## Minimum Equipment Required

The minimum equipment required for analysis of a 68360 target system consists of the following:

- An HP 1660A/61A or HP 16550A (one or two cards) Logic Analyzer.
- The HP E2448A Preprocessor Interface, which includes the configuration files and inverse assemblers.

**Note**

The HP E2448A contains eleven 16-channel pods. Six of the pods are required for inverse assembly with state analysis. The other five pods contain additional signals which may be useful for state or timing analysis.

## Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the HP E2448A Preprocessor Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

**Caution**

To prevent equipment damage, be sure to remove power from the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. Set the switches on the preprocessor interface for the mode of operation (see page 1-4).
2. If an external BDM debugger is being used, select the power source for the BDM connector and connect the debugger to the preprocessor interface (see page 1-10).
3. Connect the logic analyzer probes to the cable connectors of the preprocessor interface as listed in table 1-1 (see page 1-6).
4. Install the preprocessor interface in the target system (page 1-8).
5. Load the appropriate logic analyzer configuration file. This also loads the appropriate default inverse assembler file (page 1-9).

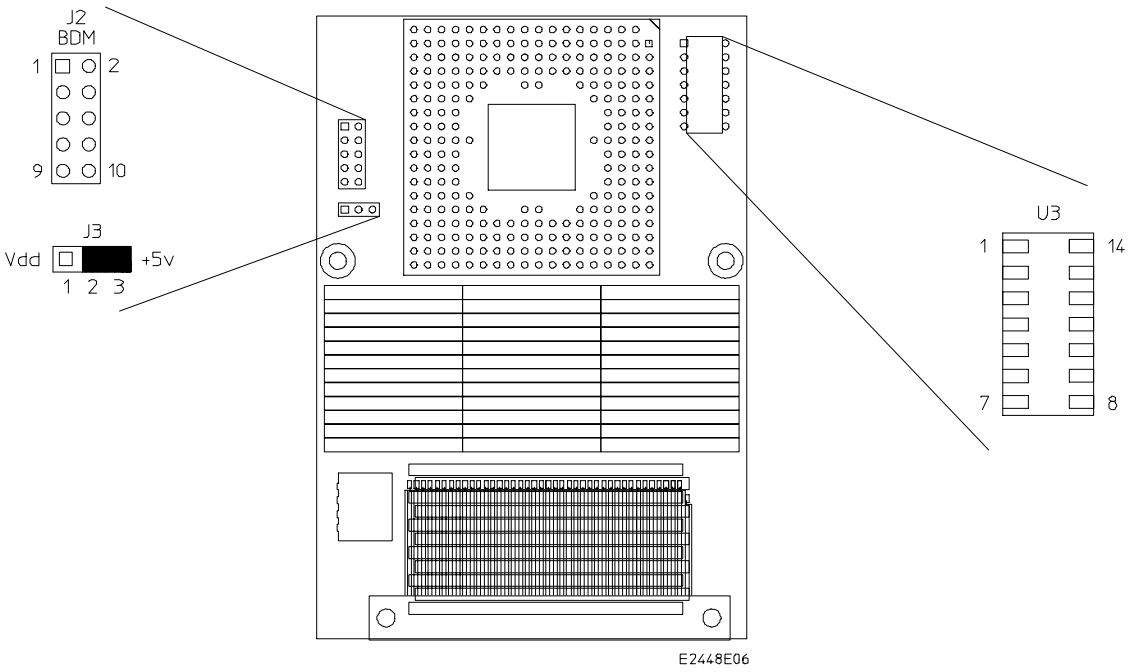


**Figure 1-1. HP E2448A Preprocessor Interface Assembly**

**Caution**

Care must be used when removing a microprocessor or socket from the preprocessor interface board to prevent damaging the traces on the board.

## Selecting the Measurement Mode

The HP E2448A Preprocessor Interface provides two state data collection modes, **Sync** and **Async**. It also provides a Timing analysis mode. The mode selected by the user will depend on the target system design and the amount of debug information desired. The modes are selected by the two outer switches of S1, and by loading the correct logic analyzer configuration file. The inner two switches of S1 are not used by the preprocessor interface.

### State Analysis

Sync mode uses the negative edge of CLK01 as a logic analyzer slave clock to capture all of the data from the preprocessor interface. When a valid bus cycle occurs, one of the following are used as logic analyzer master clocks to clock the logic analyzer: AS or DS from the 68360, or a preprocessor generated signal (show2). The Sync mode provides the most debugging information, but the target system code must enable the CLK01 output of the 68360 to use this mode. In addition to providing more debug information to the user, Sync mode operation may be required if the target does not meet the setup and hold times relative to AS or DS as specified below. The configuration files provided for Sync mode will name the analyzer machine "68360 sync."

Async mode uses the 68360 AS or DS rising edge to capture the preprocesor interface data and to clock the logic analyzer. This mode does not put any restrictions on the target code. When the Async mode is selected, the "AS only - AS/DS" switch is used to determine if AS or DS is used to capture target system read cycle information. The "AS/DS" position should only be used when the target system read data does not meet the required timing requirements relative to AS. The configuration files provided for Async mode will name the analyzer machine "68360 asyn".

**Async mode – AS only**

For Async operation, the "Sync/Async" switch must be in the Async position. In addition, there are two options which are selected with the "AS only – AS/DS" switch. The AS only position has the following characteristics:

– requires target data bus to meet 3.5/0 nsec. setup and hold relative to the rising edge of AS on read cycles.

– uses the rising edge of AS to capture the preprocessor data and to clock the logic analyzer for all bus cycles except show cycles.

– uses the rising edge of DS to capture the preprocessor data and to clock the logic analyzer on M68360 show cycles.

– will NOT capture data portion of a M68360 show cycle.

**Async mode - AS/DS** The AS/DS position for Async operation has the following characteristics:

– requires target data bus to meet 3.5/0 nsec. setup and hold relative to the rising edge of DS on read cycles.

– uses the rising edge of AS to capture the preprocessor data and to clock the logic analyzer for all bus cycle writes except show cycles.

– uses the rising edge of DS to capture the preprocessor data and to clock the logic analyzer for all bus cycle reads and show cycles.

– will NOT capture data portion of a M68360 show cycle.

– will NOT capture M68360 generated DRAM read accesses.

**Sync mode** For Sync mode, the "AS only – AS/DS" switch must be in "AS only" position. The "Sync/Async" switch must be in the Sync position. Sync operation has the following characteristics:

– requires the target code to enable the M68360 CLK01 output.

– requires target data bus to meet 0/3.5 nsec. setup and hold relative to the falling edge of the M68360 CLK01 output on read cycles.

– captures all preprocessor data on the falling edge of CLK01

– clocks the logic analyzer on all AS or DS initiated bus cycles and collects both address and data sections of a M68360 show cycle.

## Timing Analysis

All M68360 signals except for the PLL and crystal control signals are connected to the logic analyzer directly for unbuffered timing analysis. The signals excluded are EXTAL, XFC, and XTAL. The switch positions of S1 do not affect the collection of M68360 signals when using the preprocessor interface with timing analysis.

To observe the four preprocessor generated status signals (syn_cf, if_st, show1, show2), set the "Sync/Async" switch to "Sync" if the target code has enabled CLK01. Otherwise, use the "Async" mode.

## Connecting to the HP E2448A

Connect the logic analyzer probes to the cable connectors of the preprocessor interface board as listed in table 1-1. Figure 1-2 shows the relative locations of the HP 16550A Logic Analyzer cards.

## Power Up / Down Sequence

When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system.

When powering down, power down the target system first, and then the logic analyzer.

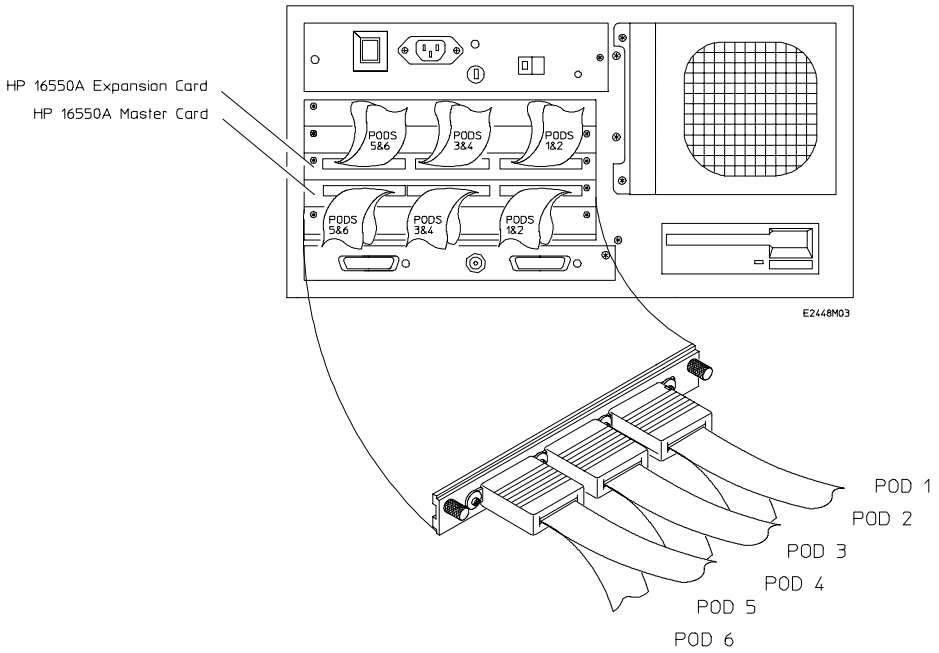


**Figure 1-2. HP 16550A Logic Analyzer Pod Locations**

**Table 1-3. Connections and Configuration Files**

| HP 16550A (one card) Logic Analyzer Pod | HP 16550A (two cards) Logic Analyzer Pod * | HP 1660A Logic Analyzer Pod | HP 1661A Logic Analyzer Pod | HP E2448A Connector |
|---|---|---|---|---|
| Master Card, Pod 1 | Master Card, Pod 1 | Pod 1 | Pod 1 | P1 (STAT) |
| Master Card, Pod 2 | Master Card, Pod 2 | Pod 2 | Pod 2 | P2 (STAT) |
| Master Card, Pod 3 | Master Card, Pod 3 | Pod 5 | Pod 3 | P3 (DATA) |
| Master Card, Pod 4 | Master Card, Pod 4 | Pod 6 | Pod 4 | P4 (DATA) |
| Master Card, Pod 5 | Master Card, Pod 5 | Pod 3 | Pod 5 | P5 (ADDR) |
| Master Card, Pod 6 | Master Card, Pod 6 | Pod 4 | Pod 6 | P6 (ADDR) |
| -- | Expander Card, Pod 1 | -- | -- | P7 (PORTA) |
| -- | Expander Card, Pod 2 | -- | -- | P8 (PORTB) |
| -- | Expander Card, Pod 3 | -- | -- | P9 (PORTC) |
| -- | Expander Card, Pod 4 | Pod 7 | -- | P10 (status) |
| -- | Expander Card, Pod 5 | Pod 8 | -- | P11 (status) |
| **Configuration Files, Synchronous Operation** | | | | |
| C68360_4 | C68360_5 | C68360_6 | C68360_7 | |
| **Configuration Files, Asynchronous Operation** | | | | |
| C68360_0 | C68360_1 | C68360_2 | C68360_3 | |
| **Configuration Files, Mixed Operation** | | | | |
| -- | C68360_8 | C68360_9 | -- | |

* For the HP 16550A cards, the Master Card is the lower card, and the expander card is the higher card. Note that the two HP 16550A cards must be configured as a single logic analyzer.

## Connecting to the Target System

The following steps explain how to connect the HP E2448A Preprocessor Interface to your target system:

**Caution**

To prevent equipment damage, be sure to remove power from the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. Remove the 68360 microprocessor from its socket on the target system and store it in a protected environment.

**Caution**

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin A1 (figure 1-1) on the preprocessor interface connector and the target system socket prior to inserting the connector in the socket. Also, take care to align the preprocessor interface connector with the socket on the target system so that all microprocessor pins are making contact.

2. Plug the preprocessor interface connector into the microprocessor socket on the target system.

**Note**

If the preprocessor interface connector interferes with components of the target system or if a higher profile is required, additional plastic pin guards can be added. Plastic pin guards can be ordered from Hewlett-Packard using the part number 1200-1828. However, any 241-pin PGA IC socket with a 68360 footprint and gold-plated pins can be used.

3. Plug the 68360 microprocessor into the socket of the preprocessor interface board. The socket on the preprocessor interface board is designed with low-insertion-force pins to allow you to install or remove the microprocessor with a minimum amount of force.

## Setting Up the Analyzer from the Disk

The logic analyzer can be configured for 68360 analysis by loading the appropriate configuration file. Each logic analyzer has one configuration file for synchronous operation and one file for asynchronous operation (see table 1-1). In addition, the two-card HP 16550A and the HP 1660A have configuration files for Mixed (simultaneous state and timing) analysis.

Loading a configuration file will also load a default inverse assembler file (I68360 or I68360E). The configuration software checks the logic analyzer system configuration during the load process and automatically loads the appropriate inverse assembler. To load the configuration and inverse assembler:

1. Install the flexible disk in the front disk drive of the logic analyzer.
2. Select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer configuration from disk.
4. Select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.
5. Use the knob to select the appropriate configuration file (see table 1-1).
6. Execute the load operation to load the file into the logic analyzer.

The I68360 inverse assembler is loaded by default with the HP 16550A Logic Analyzer in an HP 16500A mainframe, and with the HP 1660A/61A Logic Analyzers with software version V01.xx.

The I68360E inverse assembler contains enhanced features which use the increased capabilities of some of the logic analyzers. It is loaded by default with the HP 16550A Logic Analyzer in an HP 16500B mainframe, and with the HP 1660A/61A Logic Analyzers with software version V02.00 or higher.

There is also an example configuration file (EXAMPLE) which contains trace data that shows an example of the 68360 inverse assembler. This file can be loaded into any supported logic analyzer. To load the EXAMPLE configuration file, repeat steps 1 through 6 above, using EXAMPLE for step 5.

## Timing Analysis

The configuration loaded for state analysis may also be used for timing analysis. To configure the logic analyzer for timing analysis:

1. Load the appropriate configuration file from the disk (ensure that the file matches the position of the "Sync/Async" switch, see table 1-1).
2. Select the Configuration menu of the logic analyzer.
3. Select the Type field and select Timing.

## Using the BDM Connector

The HP E2448A Preprocessor Interface provides a connector (J2) for a BDM debugger (see figure 1-3). J2 complies with the 10-pin BDM connector specified in the "Motorola M68360 User's Manual."

The 3-pin connector J3 allows the user to select either a fixed + 5 volts or the Vcc from the M68360 processor (+ 3 or + 5) for the supply connected to pin 9 of the BDM connector J2 (see figure 1-1). Check the requirements of the BDM debugger being used to determine which J3 jumper position is required.

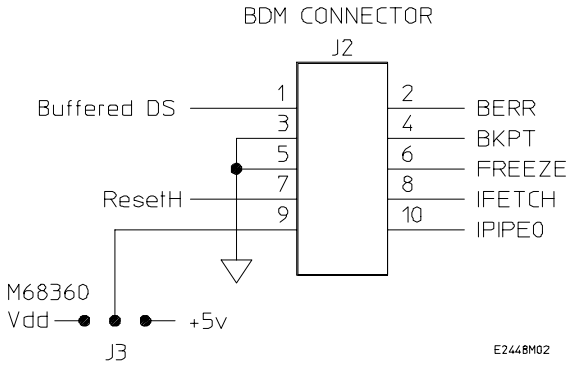


**Figure 1-3. BDM Connector**

## 68360 Clock Configuration

When the HP E2448A Preprocessor Interface is used with several stacked PGA sockets or with a flexible circuit adapter, the operation of the 68360 clock circuitry may be degraded. To correct this problem, it is possible to duplicate the target clock circuitry on the preprocessor interface by using socket U3.

The most likely problem that with be encountered will be the loss of the ability of the PLL to maintain lock due to excessive lead length in the XFC circuit. This can be remedied by adding the XFC filter to U3. Another common problem is the loss of the clock when a crystal is used. This is fixed by adding the crystal circuitry to U3.

Unless the above conditions exist, it is not necessary to install any components in the socket.

Socket U3 is connected to the 68360 clock and PLL signals to allow the circuit modification listed below. When components are added to U3 it is necessary to disconnect the leads for the corresponding signals from the target system by pushing pins out of one of the PGA sockets connected to the bottom of the Preprocessor interface. The easiest way to add components to U3 is to use a 14-pin header, rather than soldering directly to the socket.

There are five possible clock modification using U3. Any one of the five, or a combination, can be used. Table 1-2 lists the modifications, and figure 1-4 shows the pin out for U3.

**Table 1-2. Clock Configurations**

| Modification | PGA Pins to be Removed |
|---|---|
| PLL filter capacitor selection via XFC | Remove XFC pin |
| Crystal circuit with phase shift and biasing circuitry via EXTAL and XTAL | Remove EXTAL and XTAL pins |
| Oscillators. The socket layout is compatible with 14-pin DIP oscillators. | Remove EXTAL and XTAL pins |
| Termination of EXTAL line when using TTL source from target | No pins need to be removed |
| PLL configuration control via MODCK0 and MODCK1 signals | Remove MODCK0 and/or MODCK1 pins |

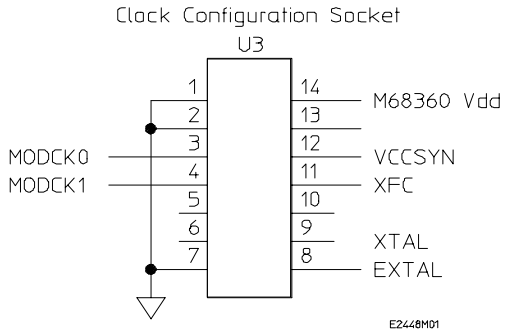


**Figure 1-4. U3 Pin Out**

The unconnected pins can be used as junction points for circuitry added to U3.

# 2

# Analyzing the Motorola 68360

## Introduction

This chapter provides reference information on the format specification and symbols configured by the HP E2448A software. It also provides information about the inverse assemblers and status encoding.

## Format Specification

When you use the HP E2448A Preprocessor Interface, the format specification set up by the software will look similar to that shown in figures 2-1 and 2-2. There are some slight differences in the displays, according to which logic analyzer you are using. Table 3-1 in chapter 3 lists the 68360 signals for the HP E2448A Preprocessor Interface and their corresponding lines to the logic analyzer.

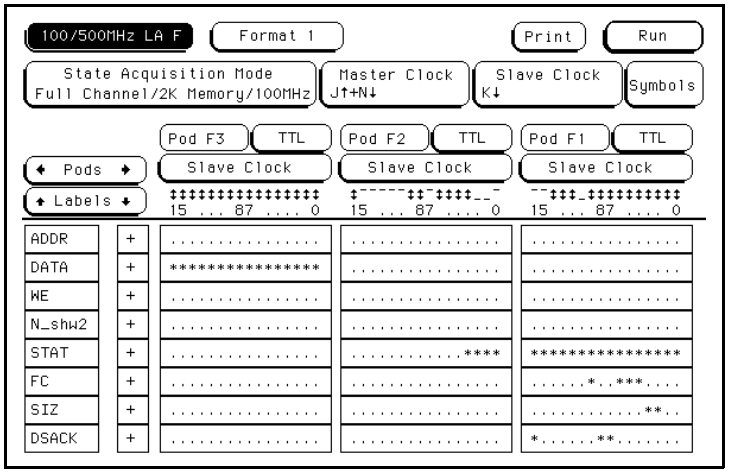


**Figure 2-1. Format Specification, Pods 1 - 3**

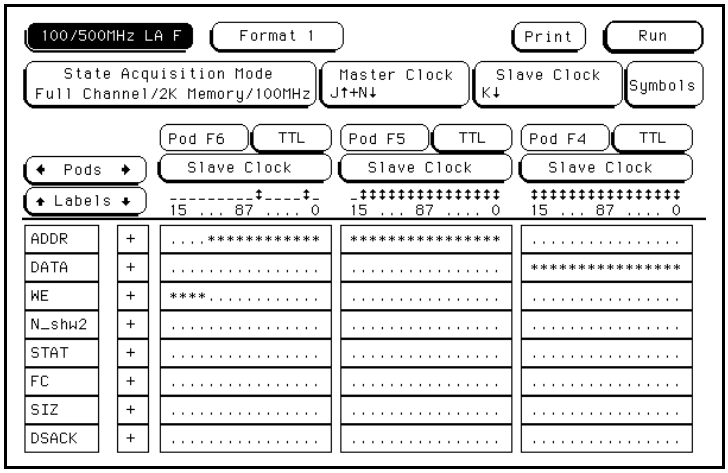


**Figure 2-2. Format Specification, Pods 4 - 6**

## Listing Menu

Captured data is displayed as shown in figure 2-3 (with the I68360 inverse assembler) or figure 2-4 (with the I68360E inverse assembler). The figures display the state listing for 32-bit bus cycles after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code. In figure 2-4, the extension words and overfetches have been suppressed.

The logic analyzers always probe the full 32-bit data bus of the 68360. There are some operations that use only 8 or 16 bits for memory transactions. The size of the bus cycle is indicated by the DSACK signals from memory to the microprocessor. When fewer than the full 32 bits of the data bus are used by a memory cycle, the inverse assembler marks the bits not used by the microprocessor with an "x."

**Note**

The "# " symbol in the state listing for the HP E2448A refers to an immediate operand.

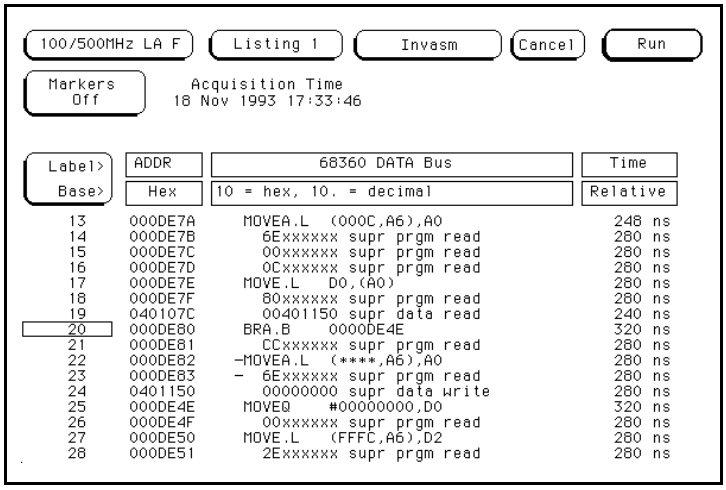


**Figure 2-3. State Listing, I68360 Inverse Assembler**

## Filtered Data With the I68360E Inverse Assembler

Figure 2-4 shows the same data as figure 2-3, with the extension words and overfetches suppressed. The suppression features are only available with the I68360E inverse assembler.

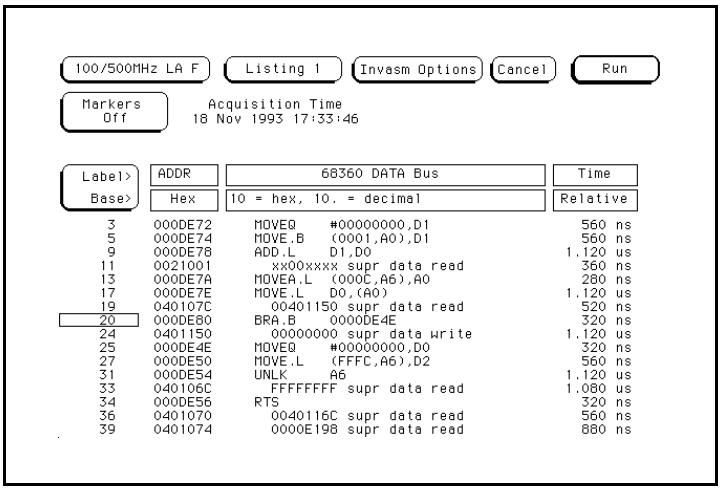


**Figure 2-4. State Listing, I68360E Inv. Assembler**

## The 68360 Inverse Assemblers

The HP E2448A Preprocessor Interface software contains two inverse assemblers, I68360 and I68360E. I68360E contains additional features which use the increased capabilities of some of the logic analyzers. For information on the I68360E features, see 'The I68360E Inverse Assembler" in this chapter.

The inverse assemblers analyze the microprocessor code and disassemble it into 68360 mnemonics, which are displayed on the logic analyzer screen. Unexecuted prefetches are marked with a hyphen (-) or question mark (?).

### Synchronizing the Inverse Assembler

The 68360 microprocessor does not provide enough status information for the inverse assembler to pick out the first word of an opcode fetch from a series of program reads. Also, in some cases the overfetch marking algorithm in the inverse assembler may lose synchronization, and unused overfetches or executed instructions may be incorrectly marked. To ensure correct disassembly, you may need to point to the 16-bit word that contains the first word of an opcode fetch. Once synchronized, the inverse assembler will disassemble from this point through the end of the screen. Use the following steps to point to the first word of an opcode fetch:

1. Select a line on the display that contains the first word of an opcode fetch.
2. Roll this line to the top of the listing.

**Note** 

The cursor location is not the top of the listing. In figure 2-3, line 13 is the top of the listing.

3. For the I68360E inverse assembler, select the "Invasm Options" field at the top of the display, then select the "Synchronize" field. For the I68360 inverse assembler, select the "Invasm" field at the top of the display and a pop-up will appear with the following choices:
   - High
   - Low

4. Select the choice that identifies which word of the 32-bit long word contains the first word of the instruction fetch. For the I68360E inverse assembler, also select "Align." The listing will inverse assemble from the top line down. Any data before this display is left unchanged.

Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the acquisition buffer by entering a new line number, or roll the screen down, you may have to re-synchronize the inverse assembler by repeating steps 1 through 4.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but activity between those blocks will not be inverse assembled.

## Interpreting Data

The instruction size for the 68360 is 16 bits. When the microprocessor is operating on a 32-bit bus, instructions may begin in either the upper or lower word (16 bits) of the captured long word (32 bits). In this case, the inverse assembler generates the least significant hexadecimal digit of the instruction address.

The inverse assembler displays most data in hexadecimal format. When data is displayed in decimal format, it has a period (.) suffix.

The pair of asterisks (**) displayed in the operand field of an instruction indicates that a byte of an expected operand was not stored in the logic analyzer memory. Four asterisks (****) indicate that one word of an expected operand was missing, and eight asterisks signify a missing long word. Missing operands (or parts of operands) can result from 68360 instruction prefetch activity or storage qualification.

**Examples:**

| | | |
|---|---|---|
| ORI.B | # **,D2 | (missing byte operand) |
| ORI.W | # ****,D1 | (missing word operand) |
| ORI.L | # 234A****,D3 | (missing "lower" word of the operand) |
| ORI.L | # ********,D3 | (missing both words of the operand) |

The 68360 is capable of supporting byte, word, and long word (32-bit) operands. During operand reads and writes, entire 32-bit values appear on the microprocessor data bus. In the case of single-byte operands, the inverse assembler will display "xx" for the bytes of the input data that are ignored by the microprocessor. In this manner, it is possible to determine exactly which byte of data the microprocessor has used as an operand.

When the 68360 is operating in a full 32-bit environment, it is possible that two instructions (16 bits each) will be fetched on one bus cycle. When this happens, the instructions will be displayed on separate lines.

## Unexecuted Prefetches

The 68360 microprocessor is a prefetching microprocessor. That is, it fetches up to three instruction words while the last opcode is still being executed. When a program executes an instruction that causes a branch, prefetched words are not used and will be discarded by the microprocessor. These words are called "Overfetches." Overfetch is indicated by the prefix "-" (hyphen) or "?" (question mark) in the inverse assembly listing.

The logic analyzer captures prefetches, even if they are not executed. Care must be taken when you are specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches at most three words, one technique to avoid unwanted triggering from unused prefetches is to add at least 8 to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

State 22 of figure 2-3 on page 2-3 is an example of a prefetched instruction which was not used. The inverse assembler could determine that the MOVEA instruction was not used since the preceding instruction, BRA.B, is an unconditional branch which always refills the instruction pipeline.

In some cases (especially with conditional branches) it is impossible to determine from bus activity whether or not a branch was taken or a prefetch was executed. In these cases, the inverse assembler will prefix the disassembled line with "?" (question mark). If there is any doubt as to whether or not an instruction was executed, it is marked "?."

The 68360 pipeline is effectively four words deep. This means that by the time a branching instruction is fully decoded, up to three other unexecuted instruction words may have already been prefetched across the data bus and stored in the logic analyzer. Both exceptions and instructions can cause the pipeline to be flushed and subsequently refilled. Branches, jumps, calls, and returns are the most common causes of pipeline flushes, but there are many others. Refer to your 68360 user's manual for more information.

## Error Messages

The following list of messages will help you identify operation errors.

**Data Error** Trace data collected by the logic analyzer cannot be retrieved from memory. This indicates a hardware error or inverse assembler software error.

**Illegal Opcode** Undefined opcode encountered. Microprocessor action cannot be determined.

---

**Note** 

Do not remove or append bits to the less significant end of the ADDR, DATA, or STAT labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Also note that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

---

## The I68360E Inverse Assembler

The I68360E inverse assembler contains additional features which use the increased capabilities of some of the logic analyzers. It supports the HP 16550A Logic Analyzer in the HP 16500B mainframe (also in the HP 16500A mainframe with software version 6.00 or higher, although not loaded by default), and the HP 1660A/61A Logic Analyzers with software version V02.00 or higher. For those logic analyzer systems, the I68360E inverse assembler is automatically loaded when the appropriate configuration file is loaded. Note that all the features in the I68360 inverse assembler are included in the I68360E inverse assembler (see previous section).

The I68360E Inverse Assembly Options menu contains two functions: display filtering with Show/Suppress selections, and Code Synchronization (see figure 2-5). The following sections describe these functions.

**Note**

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

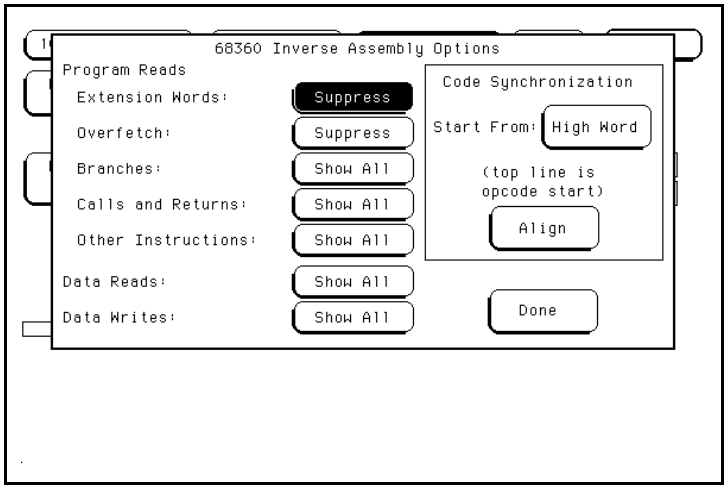


**Figure 2-5. I68360E Inverse Assembly Options**

### Show/Suppress

The Suppress/Show settings determine whether certain classes of acquisition states are shown or suppressed on the logic analyzer display. Figure 2-5 shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function allows faster analysis in two ways. First, unneeded information can be filtered out of the display. Figure 2-5 shows the settings to suppress extensions words and overfetch. Figure 2-3 (page 2-3) shows a listing with no operations suppressed. A comparison of figures 2-3 and 2-4 shows the difference in the listing display.

Second, particular operations can be isolated by suppressing all other operations. For example, memory writes can be shown, with all other operations suppressed, allowing quick analysis of memory writes.

The operations which can be shown or suppressed are User/Supervisor Reads/Writes, Program Extension states, Overfetch instructions, Branching, Call/Return, or other instructions. The Call/Return opcodes are JSR, BSR, BKPT, TRAP, RTD, RTR, RTS, RTE, STOP, and ILLEGAL. The Branching opcodes are BRA, Bcc, JMP, FBcc, TRAPcc, CHK, CHK2, and TRAPV.

### Code Synchronization

The Code Synchronization enables the inverse assembler to resynchronize with the microprocessor code. In some cases the prefetch marking algorithm in the inverse assembler may lose synchronization, and unused prefetches or executed instructions may be incorrectly marked. If any of the Code Reads are suppressed, this could cause some executed instructions to be missing from the display.

To resynchronize the inverse assembler, use the procedure on page 2-4.

### Done Field

When you are finished with the Invasm Options pop-up menu, use the Done key to return to the Listing menu.

## Symbols

The Symbol Tables of the format specification are set up with names to identify values from the 68360. Table 2-1 lists the symbols for the FC, SIZ, DSACK, BUS, R/W, RESET, and CONFIG labels, respectively. Each of the bits of the STAT label are described in table 2-2. Bit 0 is the least significant bit of the 16-bit field.

**Table 2-1. 68360 Symbols**

| Label | Symbol | Pattern |
|---|---|---|
| FC | res 0 | 0 0 0 0 |
| | udata 1 | 0 0 0 1 |
| | upgm 2 | 0 0 1 0 |
| | res 3 | 0 0 1 1 |
| | res 4 | 0 1 0 0 |
| | sdata 5 | 0 1 0 1 |
| | spgm 6 | 0 1 1 0 |
| | cpu 7 | X 1 1 1 |
| | dma 0 | 1 0 0 0 |
| | dma 1 | 1 0 0 1 |
| | dma 2 | 1 0 1 0 |
| | dma 3 | 1 0 1 1 |
| | dma 4 | 1 1 0 0 |
| | dma 5 | 1 1 0 1 |
| | dma 6 | 1 1 1 0 |
| | dma 7 | 1 1 1 1 |
| | dma | 1 X X X |
| | pgm | 0 X 1 0 |
| | data | 0 X 0 1 |
| SIZ | long | 0 0 |
| | byte | 0 1 |
| | word | 1 0 |
| | 3 byte | 1 1 |

**Table 2-1. 68360 Symbols (continued)**

| Label | Symbol | Pattern |
|---|---|---|
| DSACK | long | 0 0 |
| | byte | 0 1 |
| | word | 1 0 |
| | wait | 1 1 |
| BUS | bg_br_ack | 0 0 0 |
| | bg_br | 0 0 1 |
| | bg_ack | 0 1 0 |
| | bg | 0 1 1 |
| | br_ack | 1 0 0 |
| | br | 1 0 1 |
| | ack | 1 1 0 |
| | local | 1 1 1 |
| R/W | wrt | 0 |
| | rd | 1 |
| RESET | resS/H | 0 0 |
| | resS | 0 1 |
| | resH | 1 0 |
| | run | 1 1 |
| CONFIG | slave cs 8 3FF00 | 0 0 0 |
| | slave cs32 3FF00 | 0 0 1 |
| | slave cs16 3FF00 | 0 1 0 |
| | 68040 mode 3FF00 | 0 1 1 |
| | cpu32 cs32 3FF00 | 1 0 0 |
| | cpu32 cs16 3FF00 | 1 0 1 |
| | slave 3FF00 | 1 1 0 |
| | cpu32 3FF00 | 1 1 1 |

**Table 2-2. Status Label Bits**

| Bit | Status Signals | Description |
|---|---|---|
| 0 | BGACK | This signal is low when the microprocessor has granted control of the bus to another device. |
| 1 | R/W | This signal is high for read cycles and low for write cycles. |
| 2-3 | SIZ0-SIZ1 | These signals indicate the size of the bus transfer requested by the microprocessor. |
| 4-6, 9 | FC0-FC2, FC3 | These signals indicate the type of cycle the microprocessor is executing. |
| 7-8 | DSACK0-DSACK1 | These signals indicate the size of the bus transfer that was completed. |
| 10 | FREEZE | This signal indicates that the 68360 has acknowledged a BDM breakpoint. |
| 11-12 | IPIPE1-IPIPE0 | These signals are the 68360 instruction pipeline status. |
| 13 | IFETCH | This signal indicates that the 68360 is performing an instruction fetch. |
| 14 | PERR | This signal indicates a parity error during a read cycle. |
| 15 | BERR | This signal indicates that an erroneous bus operation is being attempted. |
| 16 | syn_cf | This signal is a preprocessor-generated signal indicating the position of the "SYNC/ASYNC" configuration switch. The inverse assembler uses this switch to validate the show2 and if_st bits described below. |
| 17 | show1 | This signal is a preprocessor generated signal indicating that this cycle is the address portion of a show cycle. |
| 18 | show2 | This signal is a preprocessor generated signal indicating that this cycle is the data portion of a show cycle. |
| 19 | if_st | This signal is a preprocessor generated signal indicating that IFETCH was asserted during this bus cycle. |

# 3

# General Information

## Introduction

This chapter contains additional reference information including the characteristics and signal mapping for the HP E2448A Preprocessor Interface.

## Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2448A Preprocessor Interface. These characteristics are included as additional information for the user.

**Microprocessor Compatibility:** Motorola 68360 and Motorola 68EN360.

**Microprocessor Package:** 241-pin PGA.

**Accessories Required:** None.

**Accessories Available:** HP E3430A Flexible Adapter.

**Maximum Clock Speed:** 33 MHz CLK.

**Target Signal Timing:** Adjustable from 3.5 ns setup/0 s hold to 0 s setup/3.5 ns hold.

**Signal Line Loading:** 25 pF in parallel with 100 KΩ to Vss for AS, DS, and CLK01.
25 pF in parallel with 10 KΩ to Vdd for FREEZE, BCLR0, RMC, TRIS, MODCK1, and MODCK0.
15 pF in parallel with 100 KΩ to Vss for all others.

**Power Requirements:** From the logic analyzer, 150 mA plus BDM current (if used) at + 5 Vdc maximum.
From the target system, microprocessor current plus BDM current (if used).

**Logic Analyzer Required:** HP 1660A/61A or HP 16550A (one or two cards) Logic Analyzer.

**Number of Probes Used:** Eleven 16-channel pods are available. Six pods are required for inverse assembly.

| | | |
|---|---|---|
| **Microprocessor Operations Displayed:** | All cycles with AS asserted<br>All cycles with DS asserted<br>All show cycles (address and data) | |
| **Additional Capabilities:** | The logic analyzer captures all bus cycles, including prefetches. Unexecuted prefetches are marked with a hyphen "–" or question mark "?." | |
| **Environmental Temperature:** | Operating: | 0 to + 55° C<br>(+ 32 to + 131° F) |
| | Nonoperating: | -40 to + 75° C<br>(-40 to + 167° F) |
| **Altitude:** | Operating: | 4,600 m (15,000 ft) |
| | Nonoperating: | 15,300 m (50,000 ft) |
| **Humidity:** | Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument. | |

## Interface Description

The primary function of the preprocessor interface is to connect the target microprocessor to the logic analyzer through the probe interface and to perform any functions unique to that particular microprocessor. The HP E2448A performs this primary function in the following ways:

- By connecting the 68360 signals directly to the logic analyzer for state or timing data collection.
- By selecting the correct logic analyzer clocks so that the data is sampled at the correct time.
- By generating additional status signals to enhance the usability of the collected data.

Figure 2-1 shows a block diagram of the HP E2448A Preprocessor Interface.

Almost all of the 68360 signals are connected directly to the logic analyzer, allowing any combination of the 68360 signals to be observed simultaneously in state and/or timing modes. The signals that are not connected include EXTAL, XTAL, and XFC.

The HP E2448A has two logic analyzer clock configurations based on the "Async" and "Sync" switch settings. When configured for "Async" mode, one master clock is used to capture the preprocessor interface data and to clock the logic analyzer. This clock is sent to the CLK signal of pod 1. The preprocessor interface hardware selects either AS or DS to be used for this clock on each bus cycle. The configuration files for "Async" mode use a setup time of 3.5 nsec and a hold time of 0 nsec.

When the "AS/DS - AS only" switch is in the "AS only" position, AS is used for the master clock on all cycles except for show cycles. For show cycles, DS is used for the capture of the address of the show cycle. The data portion of a show cycle is not captured in "Async" mode.

When the switch is in the "AS/DS" position, DS is used for the master clock for all read cycles and all show cycles. AS is the clock for all other cycles.

When operating in the "Sync" mode, the preprocessor interface generates master and slave clocks for the logic analyzer. The slave clock is the 68360 CLK01 signal connect to the CLK of pod 2. All preprocessor interface data is captured on the falling edge of CLK01.

There are two master clocks used in "Sync" mode. One is the pod 1 CLK signal used in "Async" mode, and the other is a preprocessor generated clock connected to the CLK on pod 5 (pod 3 on the HP 1660A). This clock is generated to capture the data portion of a show cycle. This clock configuration effectively uses the master clocks to qualify the slave clock data that is latched on every falling edge of CLK01. The configuration files for "Sync" mode use a setup time of 0 nsec. and a hold time of 3.5 nsec.

In addition to the 68360 signals, the preprocessor interface generates four extra status signals to enhance the ability of the inverse assembler. These signals are the four upper bits of the STATUS label (syn_cf, show1, show2 and if_st). The syn_cf signal reflects the setting of the "Async - Sync" mode switch. The inverse assembler uses syn_cf to qualify show2 and if_st, since these signals are valid only when in "Sync" mode. The signals show1 and show2 indicate to the inverse assembler when the address and data portions of a show cycle occur. The signal if_st indicates that the 68360 IFETCH signal has been asserted during the bus cycle. The inverse assembler uses if_st to eliminate incorrect instruction decoding.

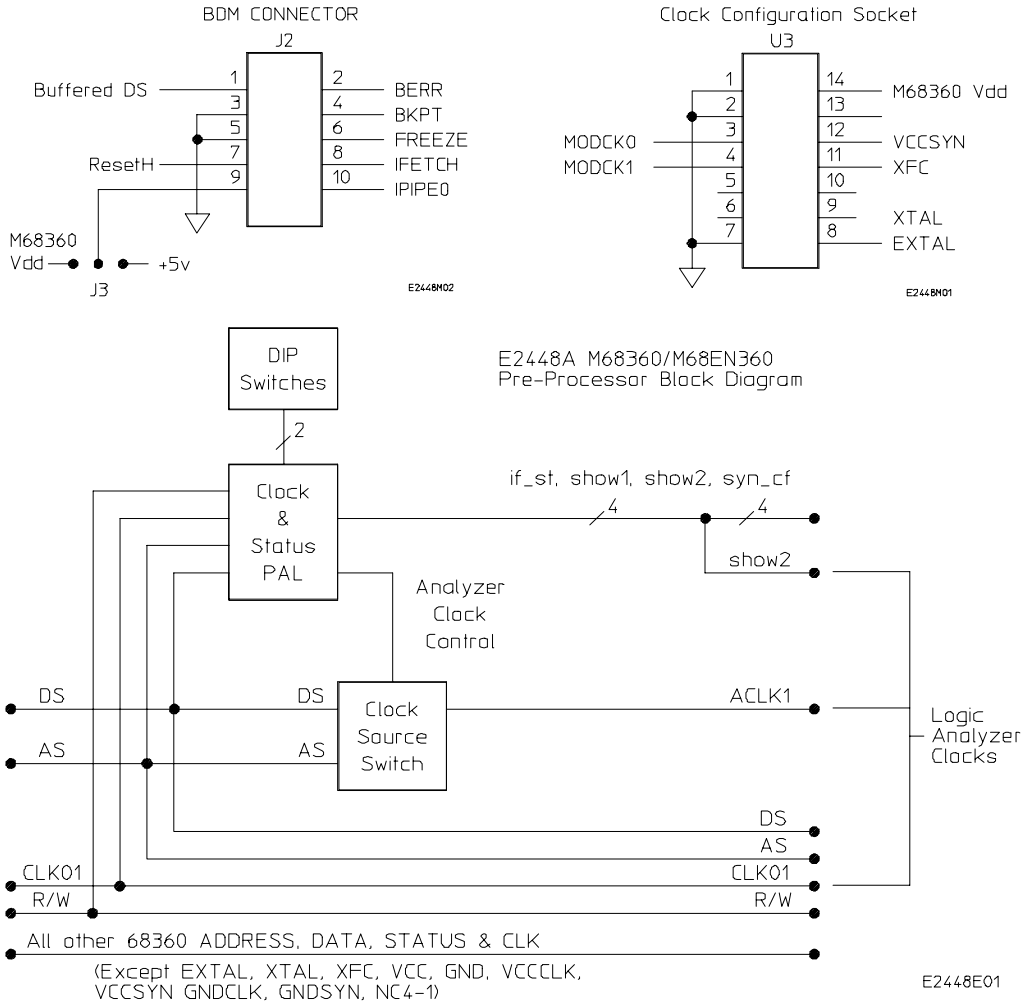


**Figure 3-1. HP E2448A Block Diagram**

## 68360 Signal to HP E2448A Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2448A Preprocessor Interface.

**Table 3-1. 68360 Signal List**

| Preprocessor Pod / Pin | Logic Analyzer Probe | 68360 PGA Pin | Pin Mnemonic | Label(s) |
|---|---|---|---|---|
| P1 / 37 | 0 | K17 | BGACK | STAT, BGACK_, BUS |
| P1 / 35 | 1 | D17 | R/W | STAT, R/W_ |
| P1 / 33 | 2 | B1 | SIZ0 | STAT, SIZ |
| P1 / 31 | 3 | C1 | SIZ1 | STAT, SIZ |
| P1 / 29 | 4 | E3 | FC0 | STAT, FC |
| P1 / 27 | 5 | D2 | FC1 | STAT, FC |
| P1 / 25 | 6 | D1 | FC2 | STAT, FC |
| P1 / 23 | 7 | D18 | DSACK0 | STAT, DSACK |
| P1 / 21 | 8 | E17 | DSACK1 | STAT, DSACK |
| P1 / 19 | 9 | E2 | FC3 | STAT, FC |
| P1 / 17 | 10 | C17 | FREEZE | STAT, FREEZE, CONFIG |
| P1 / 15 | 11 | G18 | IPIPE1 | STAT, IPIPE1 |
| P1 / 13 | 12 | G16 | IPIPE0 | STAT, IPIPE0 |
| P1 / 11 | 13 | J16 | IFETCH | STAT, IFETCH |
| P1 / 9 | 14 | P18 | PERR | STAT, PERR_ |
| P1 / 7 | 15 | Q17 | BERR | STAT, BERR_ |
| P1 / 3 | CLK | -- | -- | J_ACLK |
| P2 / 37 | 0 | * | syn_cf | STAT, syn_cf |
| P2 / 35 | 1 | * | show1 | STAT, show1 |
| P2 / 33 | 2 | * | show2 | STAT, show2 |
| P2 / 31 | 3 | * | if_st | STAT, if_st |
| P2 / 29 | 4 | G17 | AS | AS |
| P2 / 27 | 5 | C18 | DS | DS |
| P2 / 25 | 6 | H18 | OE_ | OE_ |
| P2 / 23 | 7 | P16 | HALT_ | HALT_ |

* These signals are generated by the preprocessor interface.

**Table 3-1. 68360 Signal List (Continued)**

| Preprocessor Pod / Pin | Logic Analyzer Probe | 68360 PGA Pin | Pin Mnemonic | Label(s) |
|---|---|---|---|---|
| P2 / 21 | 8 | J18 | BR_ | BR_, BUS |
| P2 / 19 | 9 | K18 | BG_ | BG_, BUS |
| P2 / 17 | 10 | L17 | BKPT_ | BKPT_ |
| P2 / 15 | 11 | N16 | AVEC_ | AVEC_ |
| P2 / 13 | 12 | M18 | RESETH_ | RESETH_, RESET |
| P2 / 11 | 13 | Q18 | RESETS_ | RESETS_, RESET |
| P2 / 9 | 14 | P17 | RMC_ | RMC_, CONFIG |
| P2 / 7 | 15 | K1 | CLK02 | CLK02 |
| P2 / 3 | CLK | J1 | CLK01 | CLK01 |
| P3 / 37 | 0 | S2 | D0 | DATA |
| P3 / 35 | 1 | R3 | D1 | DATA |
| P3 / 33 | 2 | S1 | D2 | DATA |
| P3 / 31 | 3 | R2 | D3 | DATA |
| P3 / 29 | 4 | R1 | D4 | DATA |
| P3 / 27 | 5 | Q3 | D5 | DATA |
| P3 / 25 | 6 | Q2 | D6 | DATA |
| P3 / 23 | 7 | Q1 | D7 | DATA |
| P3 / 21 | 8 | P3 | D8 | DATA |
| P3 / 19 | 9 | P2 | D9 | DATA |
| P3 / 17 | 10 | P1 | D10 | DATA |
| P3 / 15 | 11 | N3 | D11 | DATA |
| P3 / 13 | 12 | N2 | D12 | DATA |
| P3 / 11 | 13 | N1 | D13 | DATA |
| P3 / 9 | 14 | M3 | D14 | DATA |
| P3 / 7 | 15 | M2 | D15 | DATA |

**Table 3-1. 68360 Signal List (Continued)**

| Preprocessor Pod / Pin | Logic Analyzer Probe | 68360 PGA Pin | Pin Mnemonic | Label(s) |
|---|---|---|---|---|
| P4 / 37 | 0 | M1 | D16 | DATA |
| P4 / 35 | 1 | L3 | D17 | DATA |
| P4 / 33 | 2 | L2 | D18 | DATA |
| P4 / 31 | 3 | L1 | D19 | DATA |
| P4 / 29 | 4 | J2 | D20 | DATA |
| P4 / 27 | 5 | H1 | D21 | DATA |
| P4 / 25 | 6 | J3 | D22 | DATA |
| P4 / 23 | 7 | H2 | D23 | DATA |
| P4 / 21 | 8 | G1 | D24 | DATA |
| P4 / 19 | 9 | H3 | D25 | DATA |
| P4 / 17 | 10 | G2 | D26 | DATA |
| P4 / 15 | 11 | F1 | D27 | DATA |
| P4 / 13 | 12 | G3 | D28 | DATA |
| P4 / 11 | 13 | F2 | D29 | DATA |
| P4 / 9 | 14 | E1 | D30 | DATA |
| P4 / 7 | 15 | F3 | D31 | DATA |
| P5 / 37 | 0 | C12 | A0 | ADDR |
| P5 / 35 | 1 | B13 | A1 | ADDR |
| P5 / 33 | 2 | A14 | A2 | ADDR |
| P5 / 31 | 3 | A13 | A3 | ADDR |
| P5 / 29 | 4 | C11 | A4 | ADDR |
| P5 / 27 | 5 | B12 | A5 | ADDR |
| P5 / 25 | 6 | A12 | A6 | ADDR |
| P5 / 23 | 7 | B11 | A7 | ADDR |

**Table 3-1. 68360 Signal List (Continued)**

| Preprocessor Pod / Pin | Logic Analyzer Probe | 68360 PGA Pin | Pin Mnemonic | Label(s) |
|---|---|---|---|---|
| P5 / 21 | 8 | C10 | A8 | ADDR |
| P5 / 19 | 9 | A11 | A9 | ADDR |
| P5 / 17 | 10 | B10 | A10 | ADDR |
| P5 / 15 | 11 | A10 | A11 | ADDR |
| P5 / 13 | 12 | A9 | A12 | ADDR |
| P5 / 11 | 13 | B9 | A13 | ADDR |
| P5 / 9 | 14 | C9 | A14 | ADDR |
| P5 / 7 | 15 | A8 | A15 | ADDR |
| P5 / 3 | CLK | -- | -- | N_shw2 * (HP 16550, 1661) |
| P5 / 3 | CLK | -- | -- | L_shw2 * (HP 1661) |
| P6 / 37 | 0 | B8 | A16 | ADDR |
| P6 / 35 | 1 | C8 | A17 | ADDR |
| P6 / 33 | 2 | A7 | A18 | ADDR |
| P6 / 31 | 3 | B7 | A19 | ADDR |
| P6 / 29 | 4 | C7 | A20 | ADDR |
| P6 / 27 | 5 | A6 | A21 | ADDR |
| P6 / 25 | 6 | B6 | A22 | ADDR |
| P6 / 23 | 7 | C6 | A23 | ADDR |

* This is the same signal as show2 on Pod 2.

**Table 3-1. 68360 Signal List (Continued)**

| Preprocessor Pod / Pin | Logic Analyzer Probe | 68360 PGA Pin | Pin Mnemonic | Label(s) |
|---|---|---|---|---|
| P6 / 21 | 8 | A5 | A24 | ADDR |
| P6 / 19 | 9 | B5 | A25 | ADDR |
| P6 / 17 | 10 | A4 | A26 | ADDR |
| P6 / 15 | 11 | C5 | A27 | ADDR |
| P6 / 13 | 12 | B2 | A28/WE3 | WE, ADDR * |
| P6 / 11 | 13 | C2 | A29/WE2 | WE, ADDR * |
| P6 / 9 | 14 | D3 | A30/WE1 | WE, ADDR * |
| P6 / 7 | 15 | E4 | A31/WE0 | WE, ADDR * |
| P6 / 3 | CLK | M17 | TCK | Ptck |
| P7 / 37 | 0 | R8 | PA0 | PORTA |
| P7 / 35 | 1 | S7 | PA1 | PORTA |
| P7 / 33 | 2 | T6 | PA2 | PORTA |
| P7 / 31 | 3 | T5 | PA3 | PORTA |
| P7 / 29 | 4 | R7 | PA4 | PORTA |
| P7 / 27 | 5 | S6 | PA5 | PORTA |
| P7 / 25 | 6 | T4 | PA6 | PORTA |
| P7 / 23 | 7 | S5 | PA7 | PORTA |
| P7 / 21 | 8 | R6 | PA8 | PORTA |
| P7 / 19 | 9 | T3 | PA9 | PORTA |
| P7 / 17 | 10 | S4 | PA10 | PORTA |
| P7 / 15 | 11 | R5 | PA11 | PORTA |
| P7 / 13 | 12 | T2 | PA12 | PORTA |
| P7 / 11 | 13 | S3 | PA13 | PORTA |
| P7 / 9 | 14 | R4 | PA14 | PORTA |
| P7 / 7 | 15 | T1 | PA15 | PORTA |

* These signals are not included in the ADDR label in the configuration files. If the 68360 is configured with these signals as address lines, they may be added to the ADDR label.

**Table 3-1. 68360 Signal List (Continued)**

| Preprocessor Pod / Pin | Logic Analyzer Probe | 68360 PGA Pin | Pin Mnemonic | Label(s) |
|---|---|---|---|---|
| P8 / 37 | 0 | R13 | PB0 | PORTB |
| P8 / 35 | 1 | S13 | PB1 | PORTB |
| P8 / 33 | 2 | T13 | PB2 | PORTB |
| P8 / 31 | 3 | R12 | PB3 | PORTB |
| P8 / 29 | 4 | S12 | PB4 | PORTB |
| P8 / 27 | 5 | T12 | PB5 | PORTB |
| P8 / 25 | 6 | R11 | PB6 | PORTB |
| P8 / 23 | 7 | S11 | PB7 | PORTB |
| P8 / 21 | 8 | T11 | PB8 | PORTB |
| P8 / 19 | 9 | R10 | PB9 | PORTB |
| P8 / 17 | 10 | S10 | PB10 | PORTB |
| P8 / 15 | 11 | T10 | PB11 | PORTB |
| P8 / 13 | 12 | T9 | PB12 | PORTB |
| P8 / 11 | 13 | S9 | PB13 | PORTB |
| P8 / 9 | 14 | R9 | PB14 | PORTB |
| P8 / 7 | 15 | T8 | PB15 | PORTB |

**Table 3-1. 68360 Signal List (Continued)**

| Preprocessor Pod / Pin | Logic Analyzer Probe | 68360 PGA Pin | Pin Mnemonic | Label(s) |
|---|---|---|---|---|
| P9 / 37 | 0 | S8 | PB16 | PORTB |
| P9 / 35 | 1 | T7 | PB17 | PORTB |
| P9 / 33 | 2 | R16 | PC0 | PORTC |
| P9 / 31 | 3 | S17 | PC1 | PORTC |
| P9 / 29 | 4 | T18 | PC2 | PORTC |
| P9 / 27 | 5 | S16 | PC3 | PORTC |
| P9 / 25 | 6 | R15 | PC4 | PORTC |
| P9 / 23 | 7 | T17 | PC5 | PORTC |
| P9 / 21 | 8 | T16 | PC6 | PORTC |
| P9 / 19 | 9 | S15 | PC7 | PORTC |
| P9 / 17 | 10 | R14 | PC8 | PORTC |
| P9 / 15 | 11 | T15 | PC9 | PORTC |
| P9 / 13 | 12 | S14 | PC10 | PORTC |
| P9 / 11 | 13 | T14 | PC11 | PORTC |
| P9 / 9 | 14 | -- | -- | |
| P9 / 7 | 15 | -- | -- | |

**Table 3-1. 68360 Signal List (Continued)**

| Preprocessor Pod / Pin | Logic Analyzer Probe | 68360 PGA Pin | Pin Mnemonic | Label(s) |
|---|---|---|---|---|
| P10 / 37 | 0 | A18 | CS0 | CS |
| P10 / 35 | 1 | C15 | CS1 | CS |
| P10 / 33 | 2 | B16 | CS2 | CS |
| P10 / 31 | 3 | A17 | CS3 | CS |
| P10 / 29 | 4 | C14 | CS4 | CS |
| P10 / 27 | 5 | B15 | CS5 | CS |
| P10 / 25 | 6 | A16 | CS6 | CS |
| P10 / 23 | 7 | C13 | CS7 | CS |
| P10 / 21 | 8 | D16 | CAS0 | CAS |
| P10 / 19 | 9 | B18 | CAS1 | CAS |
| P10 / 17 | 10 | B17 | CAS2 | CAS |
| P10 / 15 | 11 | C16 | CAS3 | CAS |
| P10 / 13 | 12 | M16 | TDI | TDI |
| P10 / 11 | 13 | N17 | TDO | TDO |
| P10 / 9 | 14 | N18 | TMS | TMS |
| P10 / 7 | 15 | L16 | TRST_ | TRST_ |

**Table 3-1. 68360 Signal List (Continued)**

| Preprocessor Pod / Pin | Logic Analyzer Probe | 68360 PGA Pin | Pin Mnemonic | Label(s) |
|---|---|---|---|---|
| P11 / 37 | 0 | R18 | IRQ1 | IRQ |
| P11 / 35 | 1 | S18 | IRQ2 | IRQ |
| P11 / 33 | 2 | R17 | IRQ3 | IRQ |
| P11 / 31 | 3 | K16 | IRQ4 | IRQ |
| P11 / 29 | 4 | Q16 | IRQ5 | IRQ |
| P11 / 27 | 5 | L18 | IRQ6 | IRQ |
| P11 / 25 | 6 | B14 | IRQ7 | IRQ |
| P11 / 23 | 7 | F18 | PRTY0 | PRTY |
| P11 / 21 | 8 | F17 | PRTY1 | PRTY |
| P11 / 19 | 9 | F16 | PRTY2 | PRTY |
| P11 / 17 | 10 | E18 | PRTY3 | PRTY |
| P11 / 15 | 11 | M17 | TCK | TCK |
| P11 / 13 | 12 | A15 | TRIS_ | TRIS_ |
| P11 / 11 | 13 | H17 | BCLRO_ | BCLRO_, CONFIG |
| P11 / 9 | 14 | B3 | MODCK0 | MODCK0 |
| P11 / 7 | 15 | C4 | MODCK1 | MODCK1 |

## Servicing

The repair strategy for the HP E2448A is board replacement. However, table 3-2 lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

**Table 3-2. Replaceable Parts**

| HP Part Number | Description |
|---|---|
| E2448-69502 | Exchange Board/Cable Assembly |
| E2448-66502 | Circuit Board/Cable Assembly |
| E2448-68701 | Software Disk Pouch |
| 1200-1828 | Pin Protector |
| 1252-3743 | Jumper |

## Dimensions

Figure 3-2 lists the dimensions for the HP E2448A circuit board. The dimensions are listed in inches and millimeters.

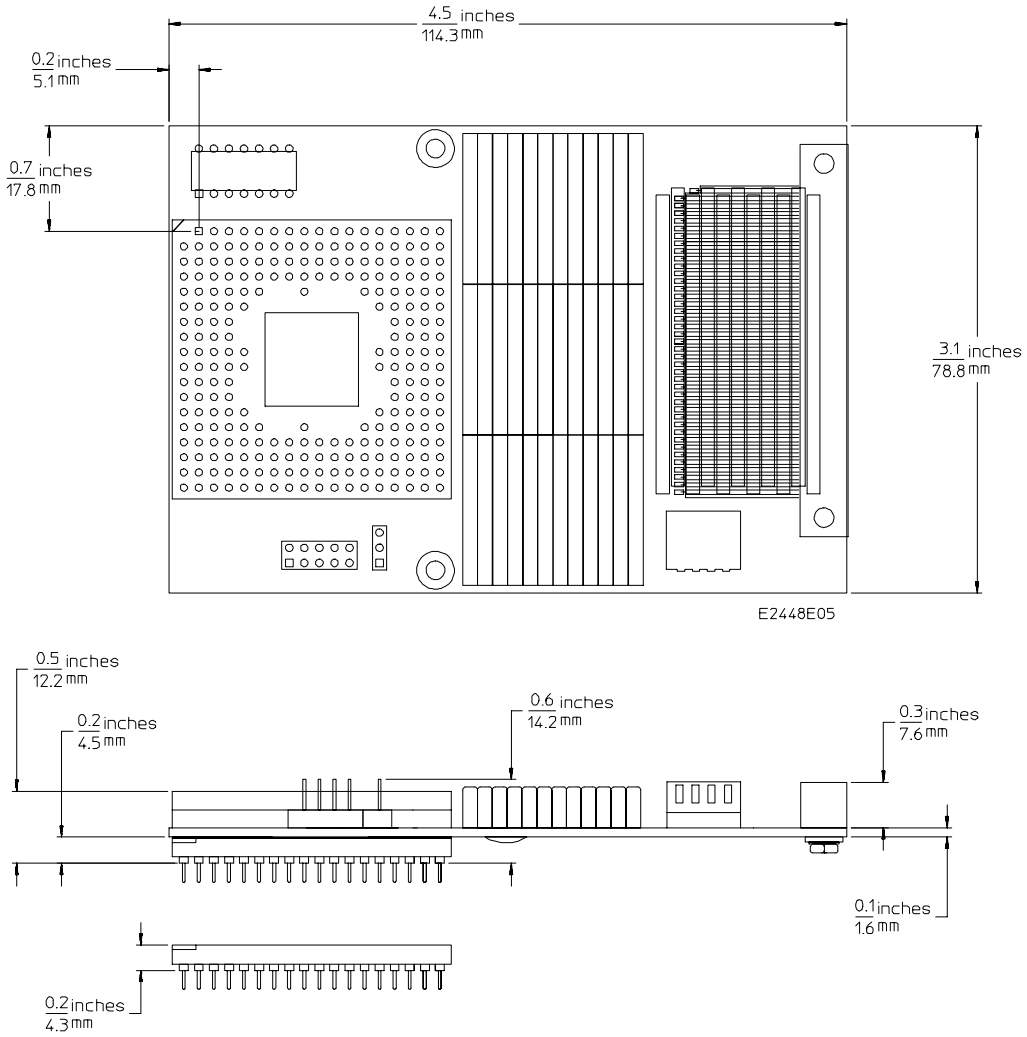


**Figure 3-2. HP E2448A Dimensions - inches/mm**

# A

# Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for assistance.

## Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").

## Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

## "Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500A/B or HP 16501A frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly. Ensure that the target system is on and operating properly.

If the error message persists, check the that the logic analyzer pods are connected to the proper connectors, as listed in table 1-1.

## Slow Clock

If you have the preprocessor interface hooked up and running and observe a slow clock or no activity from the interface board, the + 5 V supply coming from the analyzer may not be getting to the interface board.

To check the + 5 V supply coming from the analyzer, measure across pin 3 of J3 and pin 7 of U3 (see figure A-1).

- If + 5 V isn't observed across these pins, check the current limiting circuit on the logic analyzer. For information on checking this fuse or circuit, refer to the service manual for your logic analyzer.
- If + 5 V is observed across these pins and you feel confident that the + 5 V is getting to the preprocessor interface, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

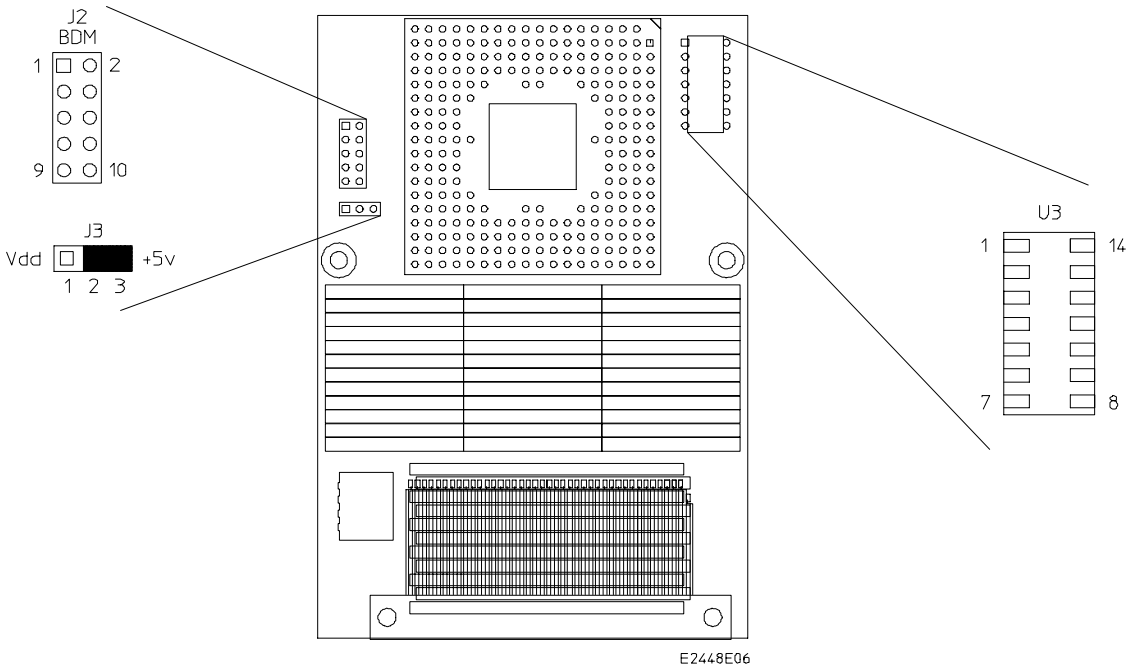


**Figure A-1. Pinout for U3 and J3**

**"No Configuration File Loaded"**

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

**"Selected File is Incompatible"**

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

**". . . Inverse Assembler Not Found"**

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

**No Inverse Assembly**

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the input cursor) and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

**Incorrect Inverse Assembly**

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file. (Note that the four additional signals can be added to the ADDR label, as mentioned on page 3-10.)
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

**No Activity on Activity Indicators**

One of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

### Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading. The following techniques will reduce the capacitive loading:

- Remove as many pin protectors, extenders, and adapters as possible.
- If multiple preprocessor interface solutions are available, try using one with lower capacitive loading.

If the clocking appears to be incorrect due to capacitive loading, try the corrective actions listed at the end of Chapter 1.

### Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

### "Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

### Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

### "Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.